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R Alverson, D Callahan, D Cummings - portal.acm.org

 ... The (LEVEL-ENTER lev) operation sets the **current privilege level** to the instruction map level if the current level is equal to lev. ...

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Hypervisor-based fault tolerance - group of 21 »

TC Bressoud, FB Schneider - ACM Transactions on Computer Systems, 1996 - portal.acm.org

Page 1. Hypervisor-Based Fault-Tolerance THOMAS C. BRESSOUD Isis Distributed Systems and FRED B. SCHNEIDER Cornell University Protocols ...

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YN Patt, SW Melvin, WM Hwu, MC Shebanow, C Chen, J ... - portal.acm.org

 ... values becomes known. The Current Mode field is a two bit field that specifies the **current privilege level** of the machine. The de ...

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Software fault tolerance in architectures with hierarchical protection levels - group of 6 »

BM Ozaki, EB Fernandez, E Gudes - doi.ieeecomputersociety.org

 ... If the descriptor denoted by the selector is visible at the **current privilege level** (the executing program has sufficient privilege to access the descriptor ...

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The design of Operating System12 - group of 4 »

MS Kogan, FL Rawson - IBM SYSTEMS JOURNAL, 1988 - research.ibm.com

 ... its descriptor. The **current privilege level** of the machine is the privilege level of the currently executing code segment. Certain ...

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16 位虚地址保护模式下 IntelX86 处理器的内存寻址机制 - group of 2 »

刘景森 - 河南大学学报 (自然科学版), 2000 - 万方数据资源系统

 ... RPL与CPL(任务当前优先级, **Current Privilege Level**)通过比较可建立

EPL(任务有效优先级, Effective Privilege Level ...

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A Multi-Threading Architecture for Multilevel Secure Transaction Processing - group of 11 »

HR Isa, WR Shockley, CE Irvine - doi.ieeecomputersociety.org

 ... for each segment. A **current privilege level** (CPL) is maintained as part of the execution state vector built into the CPU. The CPL ...

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嵌入式微处理器保护方式下高特权级系统调用的研究

聂培琴, 樊晓程, 高德远, 李树国 - 计算机学报, 2000 - 万方数据资源系统

 ... CS.selector的最低两位RPL也就成为当前运行的程序特权级CPL(**Current Privilege Level**),见图4所示. 图4 CS, SS及其高速缓存Cache. ...

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Embedded x86 Programming: Protected Mode

swipnet.se

... When entering the protected mode, the **current privilege level** (CPL) is 0 (the highest) because OS code is expected to be running. ...


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PORTING THE CHOICES OBJECT-ORIENTED OPERATING SYSTEM TO THE MOTOROLA 68030

BA HELGAAS - 1991 - choices.cs.uiuc.edu

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BY BJORN ANDREW HELGAAS BA, Augustana College, 1988 THESIS ...

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[An Extensible Protocol Architecture for Application-Specific.. - Fiuczynski \(1996\) \(Correct\) \(45 citations\)](#)
 Openness. An application, regardless of its **privilege level**, may define application-specific protocols, protocol graph that can be dynamically **changed** as applications come and go. Once in the kernel, systems does not encourage small localized **changes**. Plexus offers application developers a
www.tns.lcs.mit.edu/~djw/library/extprotarch.ps.gz

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[Just-in-time Transparent Resource Management in.. - Baratloo, Itzkovitz.. \(1998\) \(Correct\) \(1 citation\)](#)
 Furthermore, the system runs with user-level **privilege**, and thus can not compromise the security of our resource manager utilizes to dynamically **change** the allocation of resources to running jobs.
www.cs.technion.ac.il/~ayali/publications/tr1998-762.ps.gz

[A Graph-Based Network-Vulnerability Analysis System - Laura Painton Swiler \(1997\) \(Correct\)](#)
 the attacker has accessed and the user **privilege level** he or she has compromised. The arcs in the modification of access control. Edges represent a **change** of state caused by a single action taken by the and therefore, each edge represents a **change** in state on one or more devices. Examples of
infoserve.sandia.gov/sand_doc/1997/973010-1.pdf

[Optimal Charging of Capacitors - Desoete, De Vos \(Correct\)](#)

The problem is stated as follows: how to **change** the voltage $V_h(t)$ over a capacitor (with
 The challenge is the following: how to **change** the voltage source $V_c(t)$ in order to do better pin, but instead to the bulk pin. Only a dramatic **change** of technology would avoid this problem. A
www.it.dtu.dk/~jan/patmos98/papers/desoete.pdf

[IBM Secureway Cryptographic Products IBM 4758 PCI.. - First Edition June \(Correct\)](#)

. 3-14 **Privilege levels** .3-15 CP/Q

.4-1 **Privilege change** .

share underlying physical storage, in which case **changes** made by one process are visible in all other
www6.software.ibm.com/software/cryptocards/lsldesgd.pdf

[Instruction Set Commutivity - Windley \(Correct\)](#)

whether or not interrupts are enabled, and the **privilege level** of the CPU. 3 The Instruction Set. AVM-2 critical applications since reordering can easily **change** the meaning and an instruction sequence and about the rules that he gave for avoiding semantic **changes** one researcher, who developed the code
lal.cs.byu.edu/pub/hol/lal-papers/inst-comm.ps

[User-Level Threads on a General Hardware Interface - Mayes, Quick, Warboys \(1995\) \(Correct\)](#)

setregctx(pair requires a **change** in **privilege level**. 3. what facilities the processor provides
 hwo getregctx(hwo setregctx(pair requires a **change** in **privilege level**. 3. what facilities the 0 stack as the event cb. On an event, there is a **change** to **privilege-level 0** and the stack pointer is
ftp.cs.man.ac.uk/pub/cnc/arena-threads.ps.gz

[Application of Object-Oriented and Artificial Intelligence.. - Wohlrab \(1996\) \(Correct\)](#)

the frequent crossing of address space and **privilege level** boundaries turned out to be rather too 94]Other solutions are needed if requirements **change** at runtime, as it is easily the case with server modified, and, if problems arise on behalf of the **change**, the problem is fixed. The fixation can again
www.tu-chemnitz.de/informatik/HomePages/Betriebssysteme/publications/local/papers/1996/Wohlrab1996b.ps.gz

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1 [Hypervisor-based fault tolerance](#)



T. C. Bressoud, F. B. Schneider

 December 1995 **ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles SOSP '95**, Volume 29
Issue 5

Publisher: ACM Press

Full text available: [pdf\(1.26 MB\)](#)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

2 [The Tera computer system](#)



Robert Alverson, David Callahan, Daniel Cummings, Brian Koblenz, Allan Porterfield, Burton Smith

 June 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 4th international conference on Supercomputing ICS '90**, Volume 18 Issue 3b

Publisher: ACM Press

Full text available: [pdf\(746.55 KB\)](#)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

3 [Run-time generation of HPS microinstructions from a VAX instruction stream](#)



Y. N. Patt, S. W. Melvin, W. M. Hwu, M. C. Shebanow, C. Chen

 December 1986 **ACM SIGMICRO Newsletter , Proceedings of the 19th annual workshop on Microprogramming MICRO 19**, Volume 17 Issue 4

Publisher: ACM Press

Full text available: [pdf\(808.93 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The VAX architecture is a popular ISP architecture that has been implemented in several different technologies targeted to a wide range of performance specifications. However, it has been argued that the VAX has specific characteristics which preclude a very high performance implementation. We have developed a microarchitecture (HPS) which is specifically intended for implementing very high performance computing engines. Our model of execution is a restriction on fine granularity data flow. ...

4 [Hypervisor-based fault tolerance](#)



Thomas C. Bressoud, Fred B. Schneider

 February 1996 **ACM Transactions on Computer Systems (TOCS)**, Volume 14 Issue 1

**Publisher:** ACM Press

Full text available: pdf(1.89 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Protocols to implement a fault-tolerant computing system are described. These protocols augment the hypervisor of a virtual-machine manager and coordinate a primary virtual machine with its backup. No modifications to the hardware, operating system, or application programs are required. A prototype system was constructed for HP's PA-RISC instruction-set architecture. Even though the prototype was not carefully tuned, it ran programs about a factor of 2 slower than a bare machine would.

Keywords: fault-tolerant computing system, primary/backup approach, virtual-machine manager

5 [The use of microcode instrumentation for development, debugging and tuning of operating system kernels](#)



S. W. Melvin, Y. N. Patt

May 1988 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1988 ACM SIGMETRICS conference on Measurement and modeling of computer systems SIGMETRICS '88**, Volume 16 Issue 1

Publisher: ACM Press

Full text available: pdf(630.68 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We have developed a tool based on microcode modifications to a VAX 8600 which allows a wide variety of operating system measurements to be taken with minimal perturbation and without the need to modify any operating system software. A trace of interrupts, exceptions, system calls and context switches is generated as a side-effect to normal execution. In this paper we describe the tool we have developed and present some results we have gathered under both UNIX 4.3 BSD and VAX/VMS V4.5. We co ...

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